UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,211	12/01/2003	Takashi Miyazawa	117783	9841

25944 7590 06/01/2007

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
CHOW, DOON Y	
ART UNIT	**PAPER NUMBER**
2629	

MAIL DATE	DELIVERY MODE
06/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,211	MIYAZAWA, TAKASHI	
	Examiner	Art Unit	
	Dennis-Doon Chow	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-20 and 36-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-20* is/are allowed.

6)☒ Claim(s) *36-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 37-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Hiroshi (JP2003-216100).

Hiroshi discloses a method of driving an electro-optical apparatus including n rows of scanning lines each including a first subscanning line and a second subscanning line (17a2, 17c2, Fig. 118), m columns of data lines (18, Fig. 118), a power-supply line (17a1, Fig. 118), and a plurality of unit circuits arranged in n rows and m columns in association with intersections of the scanning lines and the data lines, each of the plurality of unit circuits including a first transistor (11a, Fig. 118) having a first terminal and a second terminal, a capacitor (19, Fig. 118) coupled to a first control terminal of the first transistor, a second transistor (11b, Fig. 118) that controls the electrical connection between the first terminal and the capacitor, the second transistor having a third terminal and a fourth terminal, a third transistor (11c, Fig. 118) having a fifth terminal and a sixth terminal, and an electro-optical element (15, Fig. 118)

connected to the first transistor; and a second control terminal of the second transistor being coupled to the second subscanning line of one of the n rows of scanning lines, a third control terminal of the third transistor is coupled to the first subscanning line of the one of the n rows of scanning lines, and the sixth terminal is connected to one of the m columns of data lines, the method comprising: a first step of accumulating a data signal supplied via one of the m columns of data lines in the capacitor as a charge while the second transistor and the third transistor are both on, and setting a conduction state of the first transistor according to the data signal; and a second step of turning off the third transistor and turning on the second transistor, and supplying an amount of charge that causes reduction in the conduction state, set in the first step, of the first transistor.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 36 and 40-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroshi (JP2003-216100) in view of Chen et al. (6891520)

Regarding to claims 36, 40, 41, 44-47 and 50-51, Hiroshi discloses a method of driving an electro-optical apparatus including n rows of scanning lines each including a first subscanning line and a second subscanning line (17a2, 17c2, Fig. 118), m columns

of data lines (18, Fig. 118), a power-supply line (17a1, Fig. 118), and a plurality of unit circuits arranged in n rows and m columns in association with intersections of the scanning lines and the data lines, each of the plurality of unit circuits including a first transistor (11a, Fig. 118) having a first terminal and a second terminal, a capacitor (19, Fig. 118) coupled to a first control terminal of the first transistor, a second transistor (11b, Fig. 118) that controls the electrical connection between the first terminal and the capacitor, the second transistor having a third terminal and a fourth terminal, a third transistor (11c, Fig. 118) having a fifth terminal and a sixth terminal, and an electro-optical element (15, Fig. 118) connected to the first transistor; and a second control terminal of the second transistor being coupled to the second subscanning line of one of the n rows of scanning lines, a third control terminal of the third transistor is coupled to the first subscanning line of the one of the n rows of scanning lines, and the sixth terminal is connected to one of the m columns of data lines, the method comprising: a first step of accumulating a data signal supplied via one of the m columns of data lines in the capacitor as a charge while the second transistor and the third transistor are both on, and setting a conduction state of the first transistor according to the data signal; and a second step of turning off the third transistor and turning on the second transistor, and supplying an amount of charge that causes reduction in the conduction state, set in the first step, of the first transistor.

Hiroshi does not disclose the power supply line intersects the data line.

Chen, in the same field, discloses an electro-optical apparatus comprises a power supply line (VDD, Fig. 3) and a data line (DS, Fig. 3). The power supply line intersects the data line (Fig. 3).

In light of Chen, it would have been obvious to one of ordinary skill in the art to use Chen's arrangement of the power supply line and the data line in Hiroshi's invention because this is how a power supply line and a data line are arranged in a conventional electro-optical apparatus.

Regarding to claims 42 and 48, Hiroshi further discloses a potential of the one power-supply line being set at a first voltage level, and a second voltage level different from the first voltage level being applied during at least a part of the second period.

Regarding to claims 43 and 49, Hiroshi inherently discloses the second voltage being obtained by subtracting a threshold voltage of the first transistor from the first voltage level.

5. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Allowable Subject Matter

6. Claims 18-20 are allowed.

Response to Arguments

7. Applicant's arguments filed 3/12/07 have been fully considered but they are not persuasive.

Applicant argues that Hiroshi fails to teach of suggest the first gate being electrically connected to one power supply line of the plurality of power supply line of the plurality of power supply lines during at least part of the second period. The examiner disagrees with applicant's argument. Hiroshi teaches a driving circuit having the same features as the driving circuit of the present application. For example, Fig. 118 of the Hiroshi's clearly shows the driving circuit having the same features as the driving circuit shown in the Fig. 3 of the present application. Hiroshi clearly teaches the limitations as claimed.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis-Doon Chow whose telephone number is 571-272-7767. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dennis-Doon Chow
Primary Examiner
Art Unit 2629

D. Chow
May 25, 2007